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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,527	09/01/2000	Hideo Miyake	1614.1074	7021

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EXAMINER
HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,527	MIYAKE ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Information Disclosure Statement as received on 09/10/00; Priority Document as received on 09/10/00; and Information Disclosure Statement as received on 09/24/01.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Objections

4. Claim 7 is objected to because for the following reasons: On line 26 in claim 7, it should state "execution of the basic instruction" instead of "execution of a basic instruction". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Faraboschi et al, U.S. Patent Number 5,930,508 (herein referred to as Faraboschi).

6. Referring to claim 1 Faraboschi has taught a parallel processor that performs parallel processing of one or more basic instructions contained in each of instruction words delimited by instruction delimiting information, said parallel processor comprising (Faraboschi figures 4 and 5 abstract column 3 lines 16-25):

A plurality of instruction execution units that perform processes corresponding to supplied basic instructions in parallel (Faraboschi figure 1 abstract column 3 lines 16-20 column 4 lines 46-48);

An instruction fetch unit that fetches the instruction words one by one in accordance with the instruction delimiting information (Faraboschi figure 7 column 3 lines 16-25 column 7 lines 32-36; the alignment logic 720 acts as the fetch unit); and

An instruction issue unit that selectively issues each of the basic instructions supplied from the instruction fetch unit to one of the instruction execution units to execute an issued basic instruction (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11).

7. Referring to claim 2 Faraboschi has taught wherein the plurality of instruction execution units all have the same structure (Faraboschi column 4 lines 46-50; the execution units may include two or more arithmetic units for parallel computation, and it would be inherent that the arithmetic units would perform the same functions, and does not necessarily include the multipliers since it is stated as the arithmetic units and/or multipliers).

8. Referring to claim 3 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units (Faraboschi figures 6 and 7, column 3 lines 20-25 and column 4 line 57-column 5 line 25 column 5 lines 52-60 and column 7 lines 32-44; figure 6 is represented in figure 7 by block 720, which is the alignment means, or logic, and has the same functionality as the fetch unit as described by applicant), and then supplies the rearranged basic instructions to the instruction issue unit (Faraboschi column 3 lines 23-32 and column 7 lines 37-44).

9. Referring to claim 4 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Faraboschi figure 4 reference number 740 and column 7 lines 37-44; the expansion block 740 acts as the issue unit as described by applicant).

10. Referring to claim 5 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units (Faraboschi figures 6 and 7, column 3 lines 20-25 and column 4 line 57-column 5 line 25 column 5 lines 52-60 and column 7 lines 32-44; figure 6 is represented in figure 7 by block 720, which is

the alignment means, or logic, and has the same functionality as the fetch unit as described by applicant), and then supplies the rearranged basic instructions to the instruction issue unit (Faraboschi column 3 lines 23-32 and column 7 lines 37-44); and

The instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Faraboschi figure 4 reference number 740 and column 7 lines 37-44; the expansion block 740 acts as the issue unit as described by applicant).

11. Referring to claim 6 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit fetches an instruction word that contains basic instruction arranged in advance in accordance with the arrangement of the instruction execution units (Faraboschi column 4 line 57-column 5 line 25; since the different syllables S1, S3, etc. already have the dispersal bit sets that include the functional unit where the syllable is to be executed, they are already aligned, or arranged in accordance with the execution units).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi in view of Nair et al, "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups" (herein referred to as Nair).

13. Referring to claim 7 Faraboschi has not explicitly taught wherein, depending on the type of basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of a basic instruction being currently executed is completed. However, Faraboschi has taught using different execution units to perform different functions (Faraboschi column 4 lines 46-53; arithmetic units and multipliers). Therefore, issuing the basic instruction to an execution unit is dependent on the type of basic instruction that is performed by the execution unit. Also Faraboschi taught a buffer to hold the basic instructions awaiting the execution unit (Faraboschi figure 7 reference number 750), where the buffer holds the basic instructions issued by the processor before the execution is completed with the current instruction. Nair has taught has taught wherein, depending on the type of basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of a basic instruction being currently executed is completed (Nair page 18 column 2 line 2-page 19 column 2 line 1; Nair teaches that each functional unit performs only a subset of all operations performed by the processor; Nair also teaches that scheduling instructions basically involves examination of resources needed by each instruction, so that if some resources are available to begin execution on the next instruction if those are the resources required by the next instruction, even if the previous instruction is still executing; this goes along with the teaching of the Applicant on pages 12-13 from which claim 7 is assumed to have originated from). It would have been obvious to

one of ordinary skill in the art at the time of the invention to combine the teachings of Nair with the teachings of Faraboschi to issue instructions based on the type of instruction before a previous instruction is done executing. Issuing instructions before the previous instruction is completed is known as pipelining, or sometimes micro- pipelining, and increases throughput of the execution units since the instructions do not have to wait for the previous instruction to completely finish before starting execution. Also, by having certain execution units perform a subset of all the functions of the processor, the plurality of execution units take up less space, since it does not require all of the functionalities to perform all of the functions of the processor (Nair page 18 column 2 paragraph 1-2). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to issue an instruction to a execution unit designated for certain operations, and to issue instructions before the previous instruction is completed to decrease complexity of the execution units to save production costs, and to increase throughput which reduces execution time, respectively.

14. Referring to claim 8 the combination of Faraboschi and Nair has taught wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues the supplied basic instruction before the execution of the basic instruction being currently executed is completed (Nair page 19 column 2 lines 1-8; Nair teaches that if an instruction is dependent on data currently being executed, that is not issued, but if it is not dependent on the instructions currently being executed, then the instruction is issued).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Shang et al., U.S. Patent Number 5,941,980, has taught an apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system.

Hampapuram et al., U.S. Patent Number 5,787,302, has taught software for producing instructions in a compressed format for a VLIW processor.

Johnson et al., U.S. Patent Number 5,758,114, has taught a high speed instruction alignment unit for aligning variable byte-length instructions according to predecode information in a superscalar microprocessor.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

January 30, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100